



RESPONSE UNDER 37 C.F.R. 1.116 -
EXPEDITED PROCEDURE
EXAMINING GROUP 2829

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/099,641
Applicants: : Wilbur G. Catabay and Richard Schinella
Filed: : March 15, 2002
Title : LOW K DIELECTRIC COMPOSITE LAYER FOR INTEGRATED
CIRCUIT STRUCTURE WHICH PROVIDES VOID-FREE LOW K
DIELECTRIC MATERIAL BETWEEN METAL LINES WHILE
MITIGATING VIA POISONING

Grp./ A.U. : 2829
Examiner : Lisa A. Kilday
Docket No. : 99-102/1D

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TECHNOLOGY CENTER 2829

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450	
on	September 16, 2003 (Date of Deposit)
John P. Taylor, Reg. No. 22,369	
	<i>John P. Taylor</i> Signature
	September 16, 2003 Date of Signature

RESPONSE TO FINAL REJECTION

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: September 16, 2003

Sir:

In response to the Final Rejection mailed July 16, 2003, please amend the application as follows: